

CLAIMS:

1. A method for performing passive voltage contrast on a silicon on insulator
2 (SOI) device comprising the steps of:

3 grinding a first portion of a substrate of said SOI device with a dimpling tool;
4 etching a second portion of said substrate of said SOI device with
5 tetramethylammonium hydroxide (TMAH) following said grinding of said SOI
6 device with said dimpling tool;

7 etching a third portion of said substrate and a portion of a box insulator of said
8 SOI device with hydrofluoric acid (HF) following said etching of said SOI device
9 with said TMAH;

10 applying a conductive coating to said etched portions of said substrate and
11 said box insulator of said SOI device;

12 applying said conductive coating to a portion of a body of said SOI device;
13 and

14 directing a beam of electrons at said SOI device to detect a secondary
15 emission from said SOI device.

1 2. The method as recited in claim 1, wherein said beam of electrons is directed at
2 a gate oxide area on said SOI device.

1 3. The method as recited in claim 2, wherein if said secondary emission results
2 in said gate oxide area appearing bright then a breakdown in said gate oxide of said
3 SOI device is indicated.

1 4. The method as recited in claim 2, wherein if said secondary emission results
2 in said gate oxide area appearing dark then a breakdown in said gate oxide of said
3 SOI device is not indicated.

- 1 5. The method as recited in claim 1, wherein said etching of said SOI device
- 2 with said HF stops at a body of said SOI device.

- 1 6. The method as recited in claim 1 further comprising the step of:
- 2 polishing said SOI device to a first metal layer.

- 1 7. The method as recited in claim 6 further comprising the step of:
- 2 gluing a dummy integrated circuit to a top surface of said SOI device.

- 1 8. The method as recited in claim 7 further comprising the step of:
- 2 removing said dummy integrated circuit following etching said SOI device
- 3 with said HF.

- 1 9. The method as recited in claim 1, wherein said conductive coating comprises
- 2 a carbon ink coating.

1 10. A silicon on insulator (SOI) device, comprising:
2 a substrate, wherein a first portion of said substrate is ground using a dimpling
3 tool, wherein a second portion of said substrate is etched using tetramethylammonium
4 hydroxide (TMAH), wherein a third portion of said substrate is etched using
5 hydrofluoric (HF) acid;
6 a box insulator overlaying said substrate, wherein a portion of said box
7 insulator is etched using said HF acid;
8 a body overlaying said box insulator; and
9 a polysilicon gate separated from said body by a gate oxide;
10 wherein a beam of electrons is directed at an area of said gate oxide to
11 determine if there is a breakdown in said gate oxide.

1 11. The SOI device as recited in claim 10, wherein said beam of electrons is
2 directed at said gate oxide area to detect a secondary emission from said SOI device.

1 12. The SOI device as recited in claim 11, wherein if said secondary emission
2 results in said gate oxide area appearing bright then a breakdown in said gate oxide of
3 said SOI device is detected.

1 13. The SOI device as recited in claim 11, wherein if said secondary emission
2 results in said gate oxide area appearing dark then a breakdown in said gate oxide of
3 said SOI device is not detected.

1 14. The SOI device as recited in claim 10, wherein said body is not etched using
2 said HF.

1 15. The SOI device as recited in claim 10, wherein a conductive coating is applied
2 to said etched portions of said substrate and said box insulator of said SOI device and
3 applied to a portion of said body of said SOI device.

1 16. A silicon on insulator (SOI) device, comprising:
2 a substrate, wherein a first portion of said substrate is ground using a dimpling
3 tool, wherein a second portion of said substrate is etched using tetramethylammonium
4 hydroxide (TMAH), wherein a third portion of said substrate is etched using
5 hydrofluoric (HF) acid;
6 a box insulator overlaying said substrate, wherein a portion of said box
7 insulator is etched using said HF acid;
8 a body overlaying said box insulator; and
9 a contact interconnecting said body to a metal layer;
10 wherein a beam of electrons is directed at an area of said contact to determine
11 if said contact is open.

1 17. The SOI device as recited in claim 16, wherein said beam of electrons is
2 directed at said contact area to detect a secondary emission from said SOI device.

1 18. The SOI device as recited in claim 17, wherein if said secondary emission
2 results in said contact area appearing bright then a closed contact is detected.

1 19. The SOI device as recited in claim 17, wherein if said secondary emission
2 results in said contact area appearing dark then an open contact is detected.

1 20. The SOI device as recited in claim 16, wherein said body is not etched using
2 said HF.

1 21. The SOI device as recited in claim 16, wherein a conductive coating is applied
2 to said etched portions of said substrate and said box insulator of said SOI device and
3 applied to a portion of said body of said SOI device.

1 22. A method for making a silicon on insulator (SOI) device suitable for
2 performing passive voltage contrast comprising the steps of:
3 grinding a first portion of a substrate of said SOI device with a dimpling tool;
4 etching a second portion of said substrate of said SOI device with
5 tetramethylammonium hydroxide (TMAH) following said grinding of said SOI
6 device with said dimpling tool;
7 etching a third portion of said substrate and a portion of a box insulator of said
8 SOI device with hydrofluoric acid (HF) following said etching of said SOI device
9 with said TMAH;
10 applying a conductive coating to said etched portions of said substrate and
11 said box insulator of said SOI device; and
12 applying said conductive coating to a portion of a body of said SOI device.